We claim:

1. A method for reducing leakage current in a read only memory device, comprising the step of:

positioning a precharge phase prior to an evaluation phase during a read cycle of said read only memory device.

2. The method of claim 1, further comprising the step of terminating said precharge phase by a clock edge.

3. The method of claim 2, wherein said precharge phase lasts for approximately one-half of said read cycle.

4. The method of claim 1, wherein said precharge phase is internally timed out prior to a subsequent clock edge.

5. The method of claim 4, wherein said precharge phase is less than one-half of said read cycle.

6. A read only memory device, comprising:

one or more transistors; and

a circuit to read said one or more transistors during a read cycle, wherein said read cycle positions a precharge phase prior to an evaluation phase.

7. The read only memory device of claim 6, wherein said precharge phase is terminated by a clock edge.

8. The read only memory device of claim 7, wherein said precharge phase lasts for approximately one-half of said read cycle.

9. The read only memory device of claim 6, wherein said precharge phase is internally timed out prior to a subsequent clock edge.

10. The read only memory device of claim 9, wherein said precharge phase is less than one-half of said read cycle.

11. A method for reading a read only memory device, comprising the step of:

precharging said read only memory device during a given read cycle; and

evaluating said read only memory device following said precharging of said read only memory device during said given read cycle.

12. The method of claim 11, further comprising the step of terminating said precharge phase by a clock edge.

13. The method of claim 12, wherein said precharge phase lasts for approximately one-half of said read cycle.

14. The method of claim 11, wherein said precharge phase is internally timed out prior to a subsequent clock edge.

15. The method of claim 14, wherein said precharge phase is less than one-half of said read cycle.

16. A method for reducing leakage current in a read only memory device, comprising the step of:

precharging at least one memory column in said read only memory device during a precharge phase of a given read cycle, wherein at least one memory column is not precharged during a standby phase.

17. The method of claim 16, further comprising the step of terminating said precharge phase by a clock edge.

18. The method of claim 16, wherein said precharge phase is internally timed out prior to a subsequent clock edge.

19. A read only memory device comprised of memory columns that are connected to a precharge power supply during a precharge portion of a read cycle and are not connected to a precharge power supply during a standby mode.

20. The read only memory device of claim 19, wherein said read only memory device is further configured to terminate said precharge phase by a clock edge.

21. The read only memory device of claim 19, wherein said precharge phase is internally timed out prior to a subsequent clock edge.

22. An integrated circuit, comprising:
a read only memory device, comprising:
one or more transistors; and
a circuit to read said one or more transistors during a read cycle, wherein said read cycle positions a precharge phase prior to an evaluation phase.

23. The integrated circuit of claim 22, wherein said precharge phase is terminated by a clock edge.

24. The integrated circuit of claim 23, wherein said precharge phase lasts for approximately one-half of said read cycle.

25. The integrated circuit of claim 22, wherein said precharge phase is internally timed out prior to a subsequent clock edge.

26. The integrated circuit of claim 25, wherein said precharge phase is less than one-half of said read cycle.

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